Defense & Space Systems
Teterboro, New Jersey

HUBBLE ST ACS HARDWARE SUPPLIER & SYSTEM INTEGRATOR

AlliedSignal

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FOR MORE INFORMATION PLEASE CONTACT
PAUL MAKUS, BUSINESS DEVELOPMENT
MANAGER, AT 201-393-3060

AlliedSignal Aerospace Defense and Space Systems Is An Integral Member Of The HST Program:

- **1972 - 1977** — Conducted Trade-Off Studies and Control Systems Analysis under a MSFC Contract
- **1977 - 1982** — Developed and Integrated the Pointing Control System under Contract to LMSC
- **1982 - 1990** — Provided On-Site Personnel to GSFC to Assist in Establishing the HST Control Center and Led the Development Effort for the PCS, I&C and Safe-ing Subsystems
- **1990 -Present** — Provide On-Site Personnel to Support the MOSES and FS&S Efforts

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HST RATE GYRO ASSEMBLY (RGA)

❑ SYSTEM DESIGN

- 3 Package, 6 Gyro System 64 PM RIG Gyro with Pulse Rebalance Loops
- Dual Rate Modes
- Resolution -0.00025 Sec
- Pointing Accuracy -0.007 Sec
- Mission Life Over 15 Years

❑ PERFORMANCE CAPABILITY

• Scale Factor Stability	< 0.36 PPM/Day
• Scale Factor Non-Linearity	< 3.8 PPM
• Scale Factor Linearity Stability	< 1.9 PPM
• Alignment Stability	< 1.5 Sec
• G-Insensitive Drift Stability	< 5.2×10^{-5}
• Loop Gain Stability Over Life	< 1.08% (3 Years)
• PSD Noise (0 - 20Hz)	< 0.05 Deg/Hr RMS

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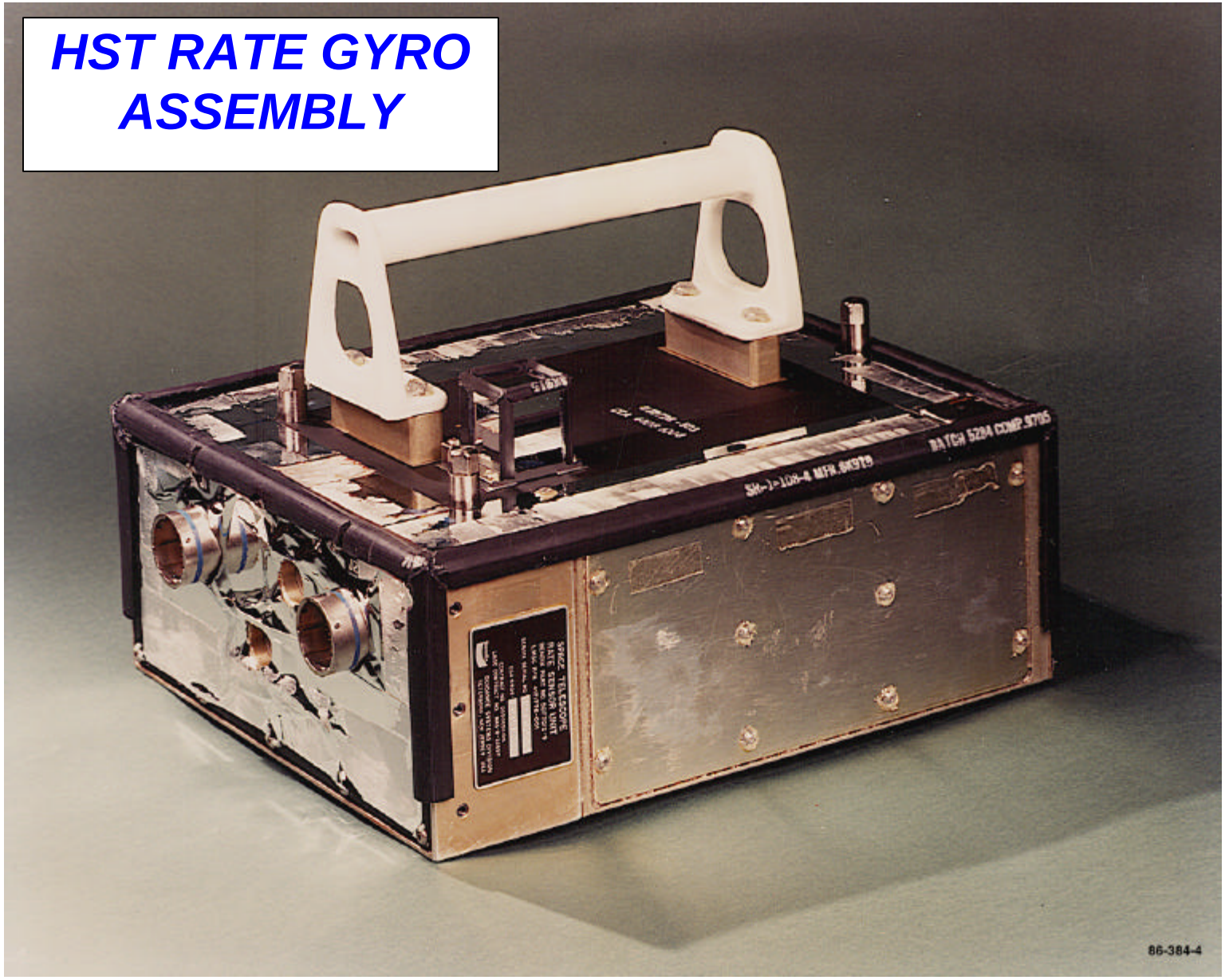
HST RATE GYRO ASSEMBLY



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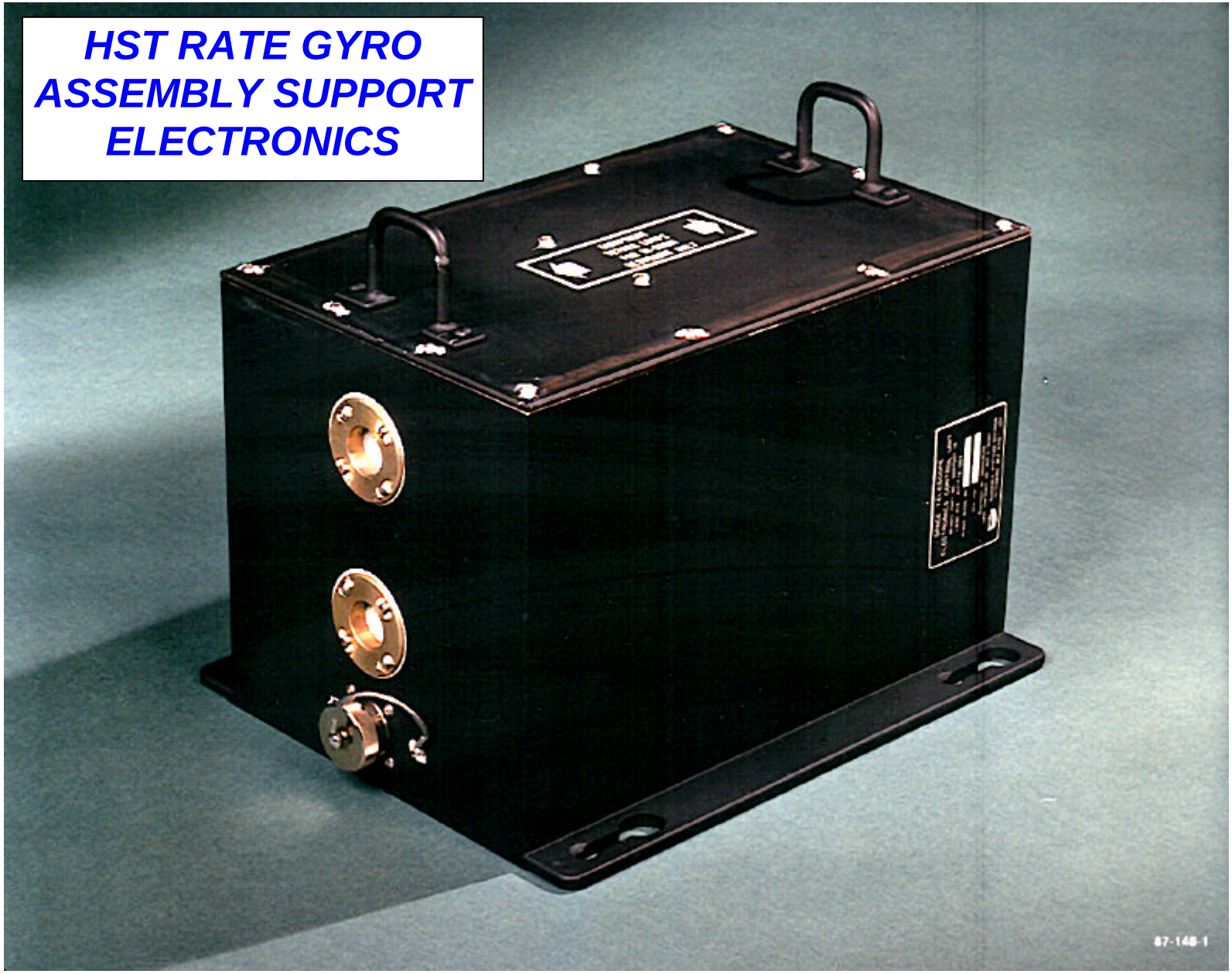
HST RATE GYRO ASSEMBLY SUPPORT ELECTRONICS



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HST POINTING & SAFEMODE ELECTRONICS ASSEMBLY (PSEA)

- **Safe Mode Functions**
  - **Autonomous safe-ing of vehicle in event of failure of Data Management System**

- **Normal Functions**
  - **Processes sun angle data for Data Management System**
  - **Monitors the health of the flight software by detecting presence of keep alive signals**

- **Physical Characteristics**
  - **Dimensions: 27" x 18" x 9"**
  - **Number of circuit card assemblies: 44**

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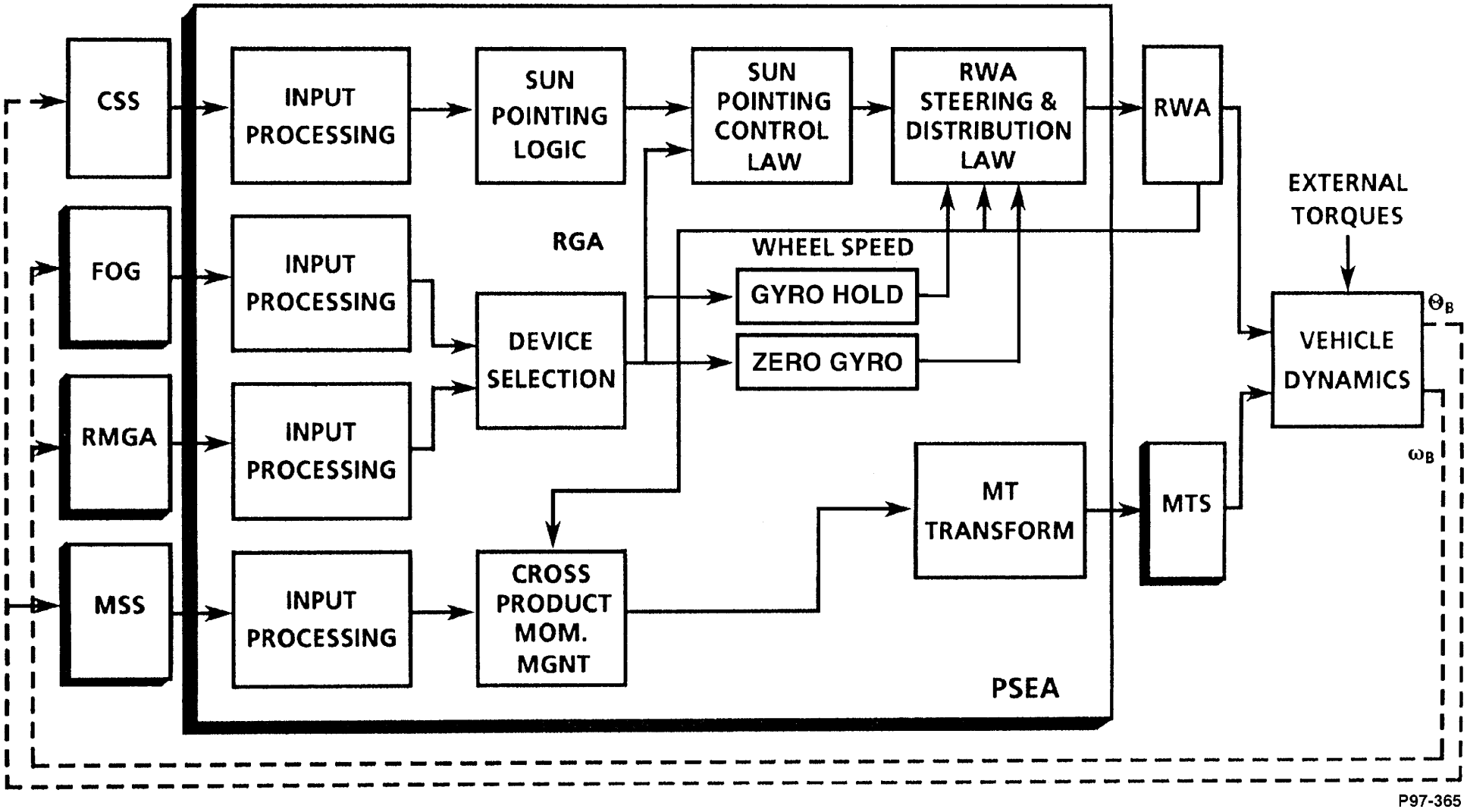

HST POINTING & SAFEMODE ELECTRONICS ASSEMBLY (PSEA)

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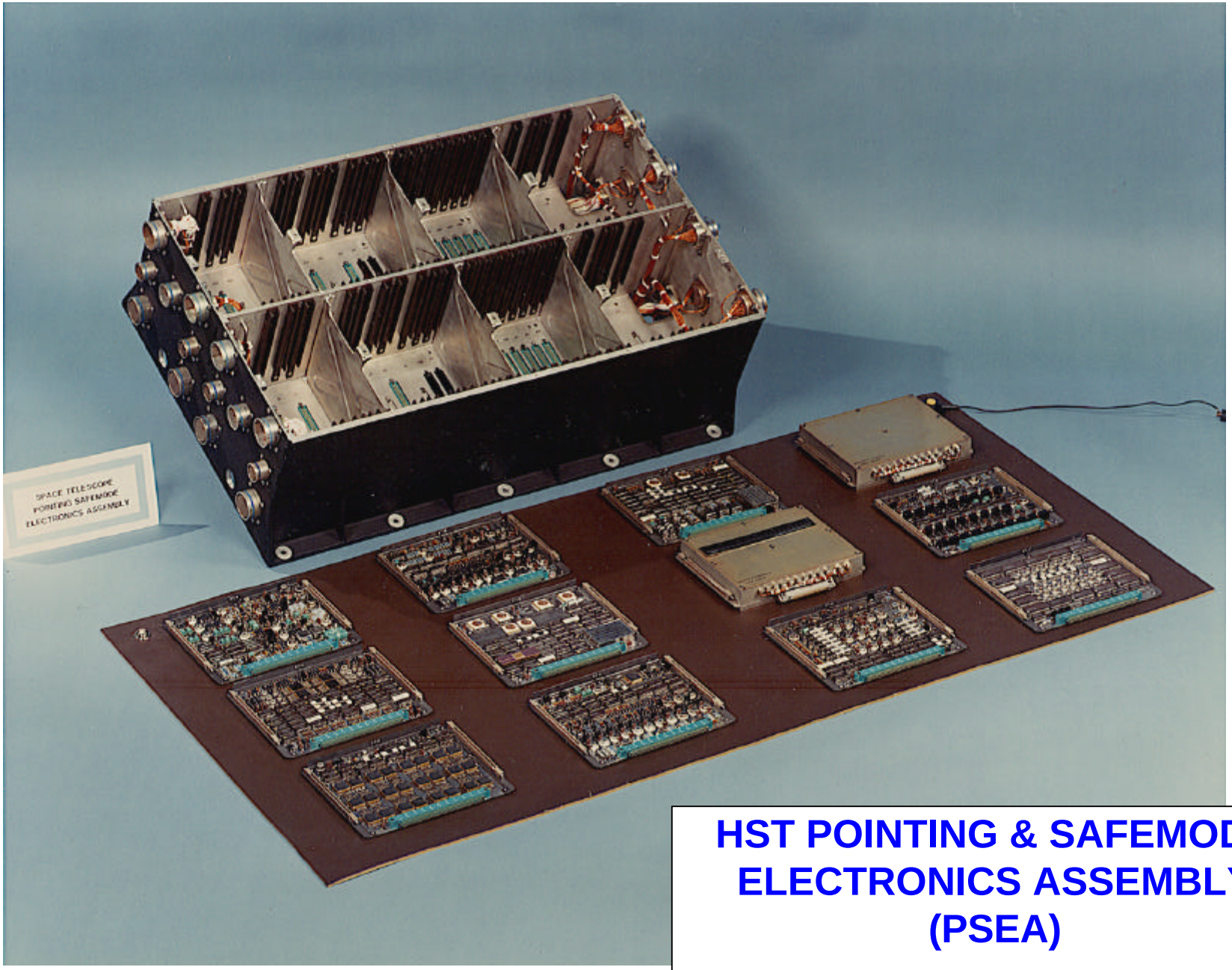

HST POINTING & SAFEMODE ELECTRONICS ASSEMBLY (PSEA)

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NEXT GENERATION POINTING & SAFEMODE ELECTRONICS ASSEMBLY

❑ Design Improvement Goals

- **10X Reduction in Size and Weight**
  - **Reduce Circuit Card Population by Miniaturization: Use of ASIC's in Place of Redundant Analog and Digital Circuitry Composed of Discrete Components**
  - **Reduce Physical Size and Weight of Housing Through Miniaturization and Light Weight Materials**

- **Hardware Design Enhancements**
  - **Upgrade Microprocessor from 8 Bits to a 32 Bit Machine**
  - **Replace Serial I/O Port with 1553B Interface**

- **Software Enhancements**

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